Amendments to the Specification

Please replace paragraph [0017] with the following amended paragraph:

[0001] The programmable divider 38 may output two differential signals, represented as A and $\bar{A}$ in Figure ~~1~~ 2. The differential outputs A and $\bar{A}$ are fed to a first input terminal of the analog mixer 40 via a series of circuit elements, including a balun transformer 44, a bandpass filter 46 and an amplifier 48, for appropriately driving the analog mixer 40. For convenience hereinafter, the output signal from the programmable divider 38 is referred to as the "loop signal."

Please replace paragraph [0018] with the following amended paragraph:

[0018] The analog mixer 40 may act as an analog phase comparator to detect the phase difference between the loop signal and a reference signal that is fed to a second input terminal of the analog mixer 40. Hence, the analog mixer 40 is referred to hereinafter as the "analog mixer phase detector 40." If the loop signal and the reference signal have the same frequency, the output error signal of the analog mixer phase detector 40 may be a DC signal whose voltage is proportional to the phase difference between the two input signals and is zero when the two signals are in phase quadrature (i.e., 90^0 out of phase). The voltage of the analog mixer phase detector 40 output signal will be a maximum positive value when the two signals are in phase and a maximum negative value when the signals are in opposite phase (i.e., 180^0 out of phase). The error signal from the analog mixer phase detector 40 is fed to the loop filter 42, which may integrate the signal from the analog mixer phase detector 40 to thereby produce the control voltage signal for the VCO ~~10~~ 32.

Please replace paragraph [0021] with the following amended paragraph:

[0021] The output pulses from the auxiliary digital frequency detector 50 are fed to a differential integrator circuit 54, which produces an output voltage, whose polarity and amplitude is proportional to the sense and magnitude, respectively, of the frequency difference between the reference signal and the comp signal, as determined by the auxiliary digital frequency detector 50. The output of the differential integrator circuit 54 may be connected to the primary timing capacitor 80 of the loop filter ~~48~~ 42, as shown in Figure 4, via a steering resistor 78.

Please replace paragraph [0022] with the following amended paragraph:

[0022] If the PLL 31 is out of lock, the auxiliary digital frequency detector 50 will detect the sense of the frequency error and will thereby cause the "steering current" to flow into or out of the loop filter timing capacitor 80. This, in turn will cause the voltage applied to the VCO ~~10~~ 32 control port to ramp up or down at a rate set by the time constant of the steering resistor 78 and the timing capacitor 80. When the VCO ~~10~~ 32 reaches a frequency such that the output signal from the analog mixer phase detector 40 is within the pass-band of the loop filter ~~48~~ 42, the PLL 31 will acquire and full phase lock may be achieved.

Please replace paragraph [0025] with the following amended paragraph:

[0025] Also as shown in Figure 4, the differential integrator circuit 54 may include an operational amplifier 72 configured as an integrator, having its inverting input connected via a resistor 74 to the "up" output signal from the auxiliary digital frequency detector 50 and having its non-inverting input connected via a resistor 76 to the "down" output signal from the auxiliary digital frequency detector 50. The output signal from the differential integrator circuit 54 may be connected to the steering resistor 78. The steering resistor 78 may be connected to the primary timing capacitor 80 of the loop filter ~~48~~ 42.

Please replace paragraph [0026] with the following amended paragraph:

[0026] As shown in Figure 4, the loop filter ~~48~~ 42 may also include an operational amplifier 82 configured as an integrator. The non-inverting input terminal of the operational amplifier 82 may be connected to a constant voltage (such as ground), and the inverting input terminal may be connected to the output terminal of the analog mixer phase detector 40. The loop bandwidth for the loop filter ~~48~~ 42 is set by the primary timing capacitor 80 and the timing resistors 84, 86. As explained previously, if the PLL 31 is out of lock, the auxiliary digital frequency detector 50 will detect the sense of the frequency error and will thereby cause the "steering current" to flow into or out of the loop filter timing capacitor 80. This, in turn will cause the voltage applied to the VCO ~~10~~ 32 control port to ramp up or down at a rate set by the time constant of the steering resistor 78 and the timing capacitor 80. When the VCO ~~10~~ 32 reaches a frequency such that the

output signal from the analog mixer phase detector 40 is within the pass-band of the loop filter ~~48~~ 42, the PLL 31 will acquire and full phase lock may be achieved.